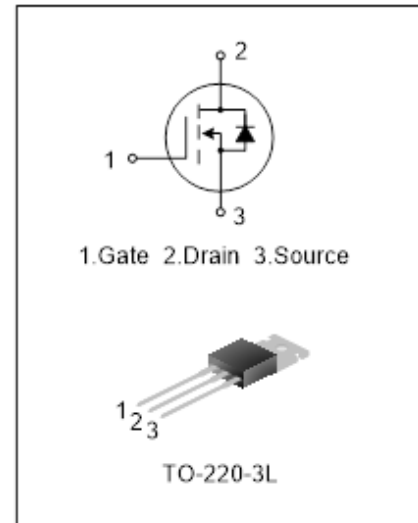


80A, 75V N-Channel MOSFET

General Description

GGVD75N08T is an N-channel enhancement mode MOS field effect transistor which is produced using Silan new structure VDMOS technology. The improved planar stripe cell and the improved guard ring terminal have been especially tailored to minimize on-state resistance, provide superior switching performance, and withstand high energy pulse in the avalanche and commutation mode. Optimize the parasitic parameters of the device and enhance the anti-jamming capability of the gate, which make it easy to use in parallel. These devices are widely used in AC-DC power suppliers, DC-DC converters and H-bridge PWM motor drivers.



Features

- 80A, 75V, RDS(on) (typ.) =9mΩ@VGS=10V
- Low gate charge
- Low Crss
- Fast switching
- Improved dv/dt capability

Ordering Information

Part No.	Package	Marking	Material	Packing
GGVD75N08T	TO-220-3L	GGVD75N08T	Pb free	Tube

Absolute Maximum Ratings (TC=25°C unless otherwise noted)

Characteristics	Symbol	Rating	Unit
Drain-Source Voltage	V _{DS}	75	V
Gate-Source Voltage	V _{GS}	±20	V
Drain Current	I _D	T _C =25°C	80
		T _C =100°C	70
Drain Current Pulsed	I _{DM}	300.0	A
Power Dissipation(T _C =25°C) -Derate above 25°C	P _D	300	W
		2.40	W/°C
Single Pulsed Avalanche Energy (Note 1)	E _{AS}	844	mJ
Operation Junction Temperature Range	T _J	-55~+150	°C
Storage Temperature Range	T _{stg}	-55~+150	°C

THERMAL CHARACTERISTICS

Characteristics	Symbol	Rating	Unit
Thermal Resistance, Junction-to-Case	$R_{\theta JC}$	0.42	$^{\circ}\text{C}/\text{W}$
Thermal Resistance, Junction-to-Ambient	$R_{\theta JA}$	62.50	$^{\circ}\text{C}/\text{W}$

ELECTRICAL CHARACTERISTICS ($T_C=25^{\circ}\text{C}$ unless otherwise noted)

Characteristics	Symbol	Test conditions	Min.	Typ.	Max.	Unit
Drain –Source Breakdown Voltage	B_{VDSS}	$V_{GS}=0\text{V}, I_D=250\mu\text{A}$	75	--	--	V
Drain-Source Leakage Current	I_{DSS}	$V_{DS}=75\text{V}, V_{GS}=0\text{V}$	--	--	1.0	μA
Gate-Source Leakage Current	I_{GSS}	$V_{GS}=\pm 20\text{V}, V_{DS}=0\text{V}$	--	--	± 100	nA
Gate Threshold Voltage	$V_{GS(th)}$	$V_{GS}=V_{DS}, I_D=250\mu\text{A}$	2	--	4.0	V
Static Drain- Source On State Resistance	$R_{DS(on)}$	$V_{GS}=10\text{V}, I_D=40\text{A}$	--	9	12	m Ω
Input Capacitance	C_{iss}	$V_{DS}=25\text{V}, V_{GS}=0\text{V}, f=1.0\text{MHz}$	--	3486	--	pF
Output Capacitance	C_{oss}		--	790	--	
Reverse Transfer Capacitance	C_{rss}		--	143	--	
Turn-on Delay Time	$t_{d(on)}$	$V_{DD}=40\text{V}, V_{GS}=10\text{V},$ $R_G=25\Omega, I_D=37.5\text{A}$ (Note 2,3)	--	55	--	ns
Turn-on Rise Time	t_r		--	229	--	
Turn-off Delay Time	$t_{d(off)}$		--	260	--	
Turn-off Fall Time	t_f		--	124	--	
Total Gate Charge	Q_g	$V_{DS}=60\text{V}, I_D=75\text{A},$ $V_{GS}=10\text{V}$ (Note 2,3)	--	93	--	nC
Gate-Source Charge	Q_{gs}		--	20	--	
Gate-Drain Charge	Q_{gd}		--	44	--	

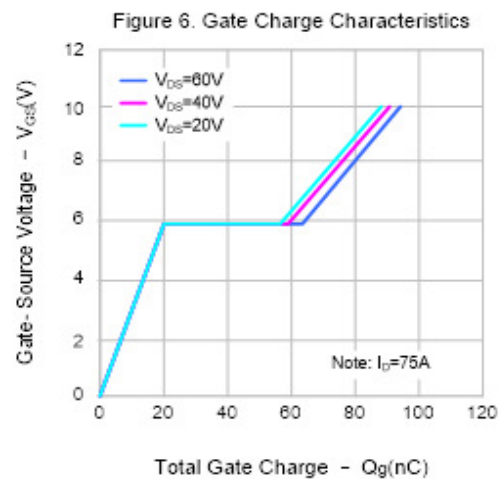
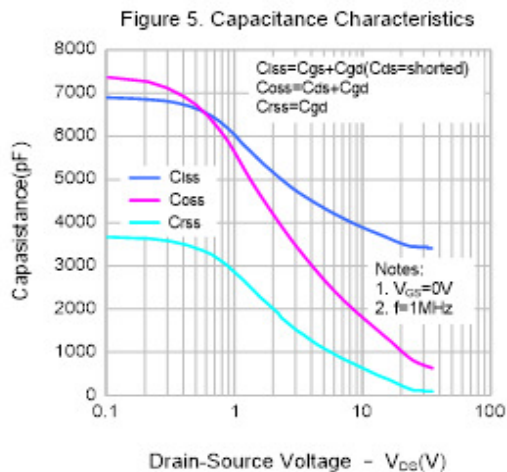
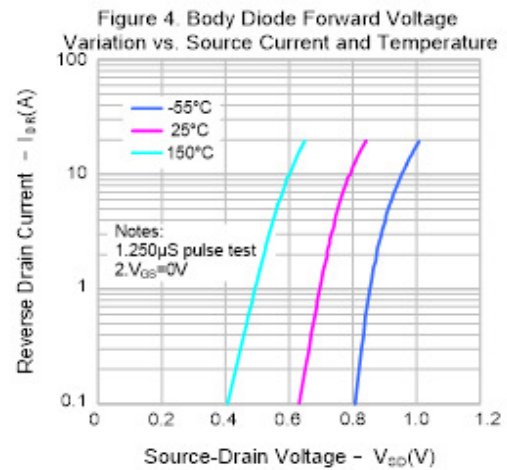
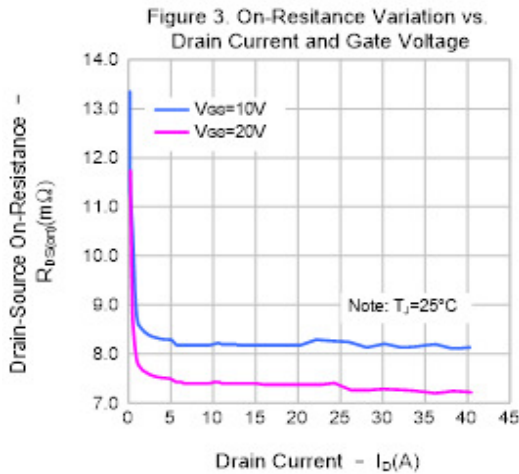
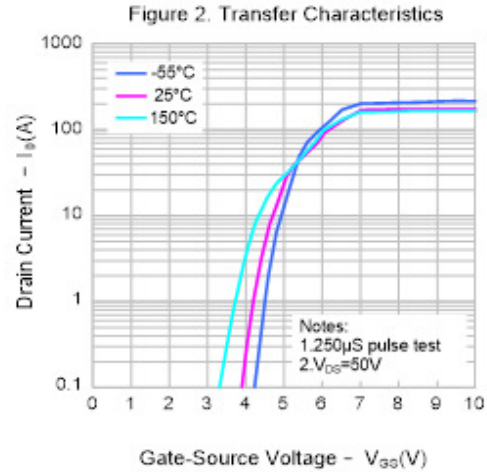
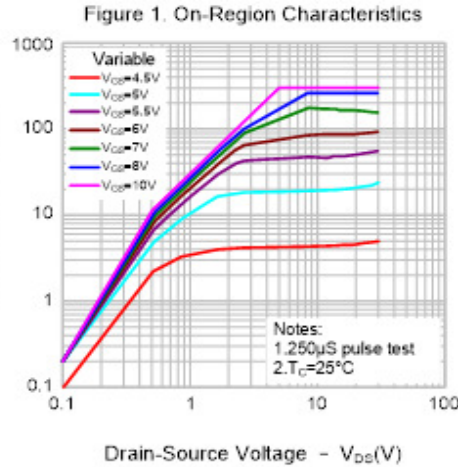
SOURCE-DRAIN DIODE RATINGS AND CHARACTERISTICS

Characteristics	Symbol	Test conditions	Min.	Typ.	Max.	Unit
Continuous Source Current	I_S	Integral Reverse P-N Junction Diode in the MOSFET	--	--	80	A
Pulsed Source Current	I_{SM}		--	--	300.0	
Diode Forward Voltage	V_{SD}	$I_S=80\text{A}, V_{GS}=0\text{V}$	--	--	1.5	V
Reverse Recovery Time	T_{rr}	$I_S=80\text{A}, V_{GS}=0\text{V},$ $dI_F/dt=100\text{A}/\mu\text{s}$ (Note 2)	--	91	--	ns
Reverse Recovery Charge	Q_{rr}		--	0.33	--	μC

Notes:

- $L=0.24\text{mH}, I_{AS}=85\text{A}, V_{DD}=35\text{V}, R_G=25\Omega$, starting $T_J=25^{\circ}\text{C}$;
- Pulse Test: Pulse width $\leq 300\mu\text{s}$, Duty cycle $\leq 2\%$;
- Essentially independent of operating temperature.

TYPICAL CHARACTERISTICS



Typical Characteristics (Continued)

Figure 7. Breakdown Voltage Variation vs. Temperature

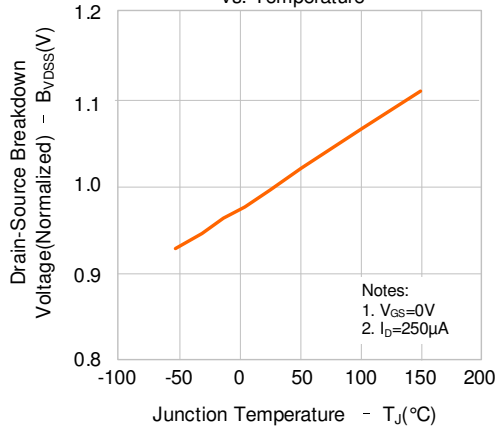


Figure 8. On-resistance Variation vs. Temperature

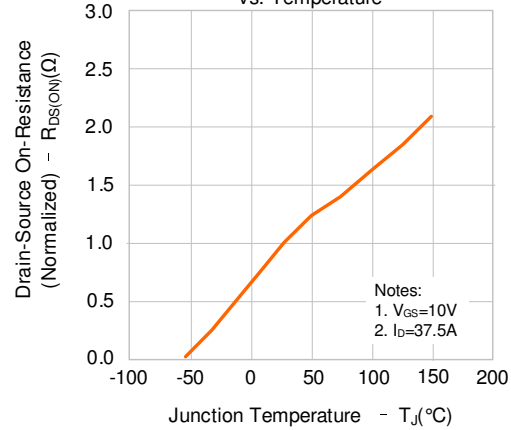
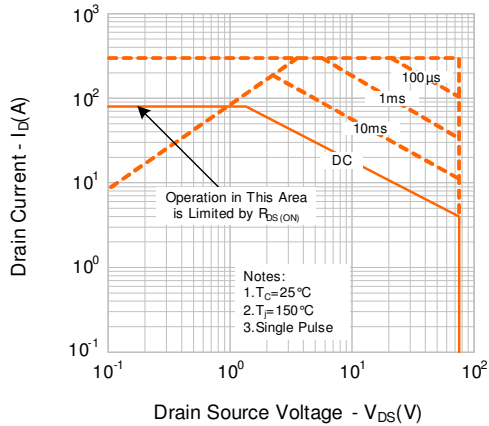
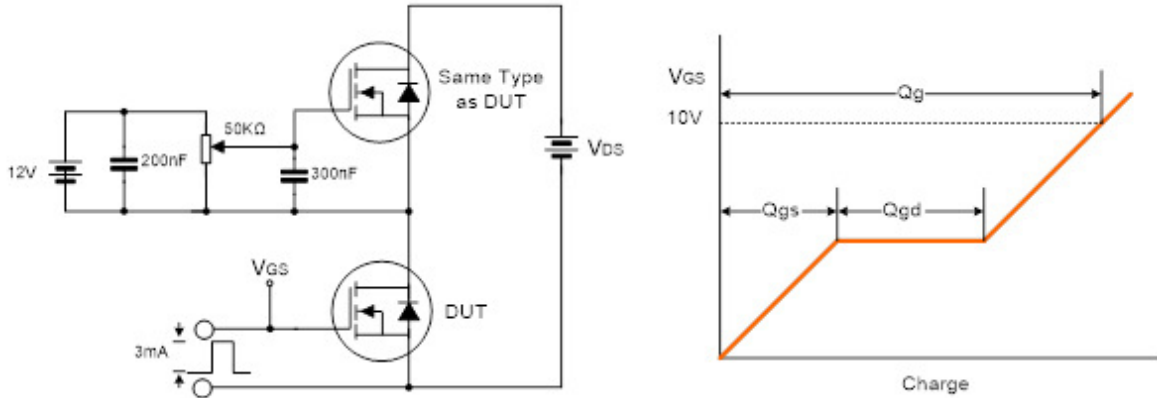


Figure 9. Max. Safe Operating Area

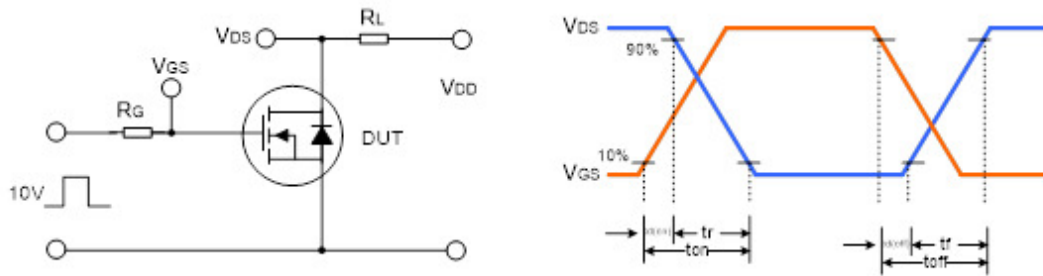


TYPICAL TEST CIRCUIT

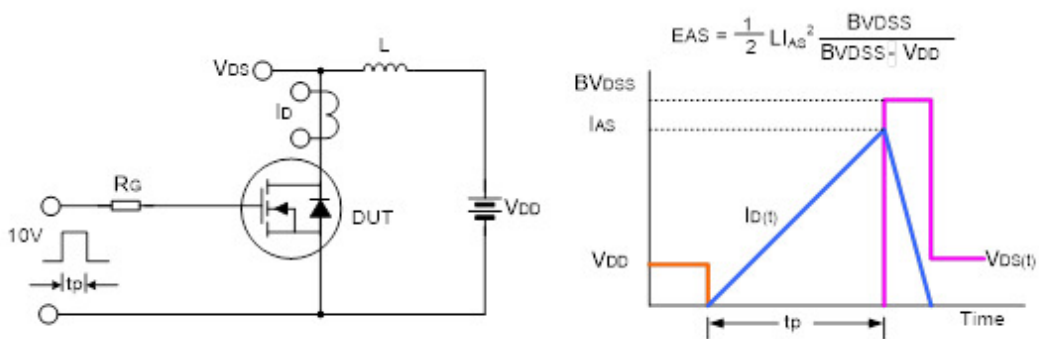
Gate Charge Test Circuit & Waveform



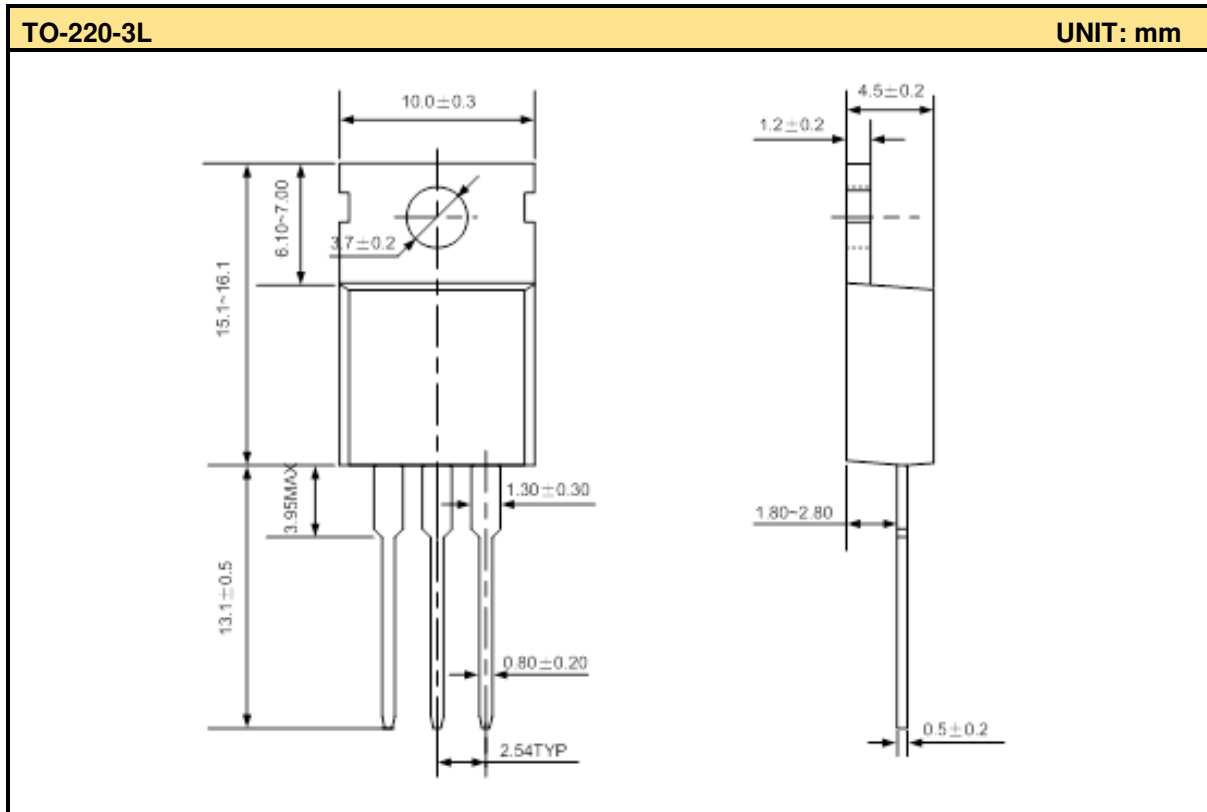
Switching Test Circuit & Waveform



EAS Test Circuit & Waveform



Package Outline



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