

57A, 100V N-Channel MOSFET

General Description

GGVD3710T is an N-channel enhancement mode power MOS field effect transistor which is produced using a proprietary version of VDMOS technology. The improved planar stripe cell and the improved guard ring terminal have been especially tailored to minimize on-state resistance, provide superior switching performance, and withstand high energy pulses in the avalanche and commutation mode.

These devices are widely used in AC-DC power supplies, DC-DC converters, and H-bridge PWM motor drivers.

Features

- 57A, 100V, $R_{DS(on)}$ (typ) = 18.4m Ω @ $V_{GS}=10V$
- Low gate charge
- Low Crss
- Fast switching
- Improved dv/dt capability

Ordering Information

Part No.	Package	Marking	Material	Packing
GGVD3710T	TO-220-3L	GGVD3710T	Pb free	Tube

Absolute Maximum Ratings ($T_C=25^\circ\text{C}$ unless otherwise noted)

Characteristics	Symbol	Rating	Unit
Drain-Source Voltage	V_{DS}	100	V
Gate-Source Voltage	V_{GS}	± 20	V
Drain Current	I_D	$T_C=25^\circ\text{C}$	57
		$T_C=100^\circ\text{C}$	40
Drain Current Pulsed	I_{DM}	230	A
Power Dissipation($T_C=25^\circ\text{C}$) -Derate above 25°C	P_D	200	W
		1.3	W/ $^\circ\text{C}$
Single Pulsed Avalanche Energy(Note 1)	E_{AS}	1060	mJ
Operation Junction Temperature Range	T_J	$-55\sim+150$	$^\circ\text{C}$
Storage Temperature Range	T_{stg}	$-55\sim+150$	$^\circ\text{C}$

Thermal Characteristics

Characteristics	Symbol	Rating	Unit
Thermal Resistance, Junction-to-Case	$R_{\theta JC}$	0.75	$^\circ\text{C}/\text{W}$
Thermal Resistance, Junction-to-Ambient	$R_{\theta JA}$	62	$^\circ\text{C}/\text{W}$

Electrical Characteristics ($T_C=25^\circ\text{C}$ unless otherwise noted)

Characteristics	Symbol	Test conditions	Min.	Typ.	Max.	Unit
Drain-Source Breakdown Voltage	$B_{V_{DS}}$	$V_{GS}=0\text{V}, I_D=250\mu\text{A}$	100	--	--	V
Drain-Source Leakage Current	I_{DSS}	$V_{DS}=100\text{V}, V_{GS}=0\text{V}$	--	--	25	μA
Gate-Source Leakage Current	I_{GSS}	$V_{GS}=\pm 20\text{V}, V_{DS}=0\text{V}$	--	--	± 100	nA
Gate Threshold Voltage	$V_{GS(th)}$	$V_{GS}=V_{DS}, I_D=250\mu\text{A}$	2.0	--	4.0	V
Static Drain-Source On State Resistance	$R_{DS(on)}$	$V_{GS}=10\text{V}, I_D=28\text{A}$	--	18.4	23	m Ω
Input Capacitance	C_{iss}	$V_{DS}=25\text{V}, V_{GS}=0\text{V},$ $f=1.0\text{MHz}$	--	3130	--	pF
Output Capacitance	C_{oss}		--	410	--	
Reverse Transfer Capacitance	C_{rss}		--	72	--	
Turn-on Delay Time	$t_{d(on)}$	$V_{DD}=50\text{V}, V_{GS}=10\text{V},$ $R_G=2.5\Omega$	--	12	--	ns
Turn-on Rise Time	t_r		--	58	--	
Turn-off Delay Time	$t_{d(off)}$		--	45	--	
Turn-off Fall Time	t_f		--	47	--	
Total Gate Charge	Q_g	$V_{DS}=80\text{V}, I_D=28\text{A}, V_{GS}=10\text{V}$	--	--	130	nC
Gate-Source Charge	Q_{gs}		--	--	26	
Gate-Drain Charge	Q_{gd}		--	--	43	

Source-Drain Diode Ratings and Characteristics

Characteristics	Symbol	Test conditions	Min.	Typ.	Max.	Unit
Continuous Source Current	I_S	Integral Reverse P-N Junction Diode in the MOSFET	--	--	57	A
Pulsed Source Current	I_{SM}		--	--	230	
Diode Forward Voltage	V_{SD}	$I_S=57A, V_{GS}=0V$	--	--	1.2	V
Reverse Recovery Time	T_{rr}	$I_S=57A, V_{GS}=0V,$ $dI_F/dt=100A/\mu s$	--	140	220	ns
Reverse Recovery Charge	Q_{rr}		--	670	1010	μC

Notes:

1. $L=0.7mH, I_{AS}=57A, V_{DD}=25V, R_G=0\Omega,$ starting $T_J=25^\circ C$;
2. Pulse Test: Pulse width $\leq 300\mu s,$ Duty cycle $\leq 2\%$;
3. Essentially independent of operating temperature.

Package Outline

TO-220-3L	UNIT: mm
[Blank area for package outline drawing]	

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